**NAME = Mukand Krishna**

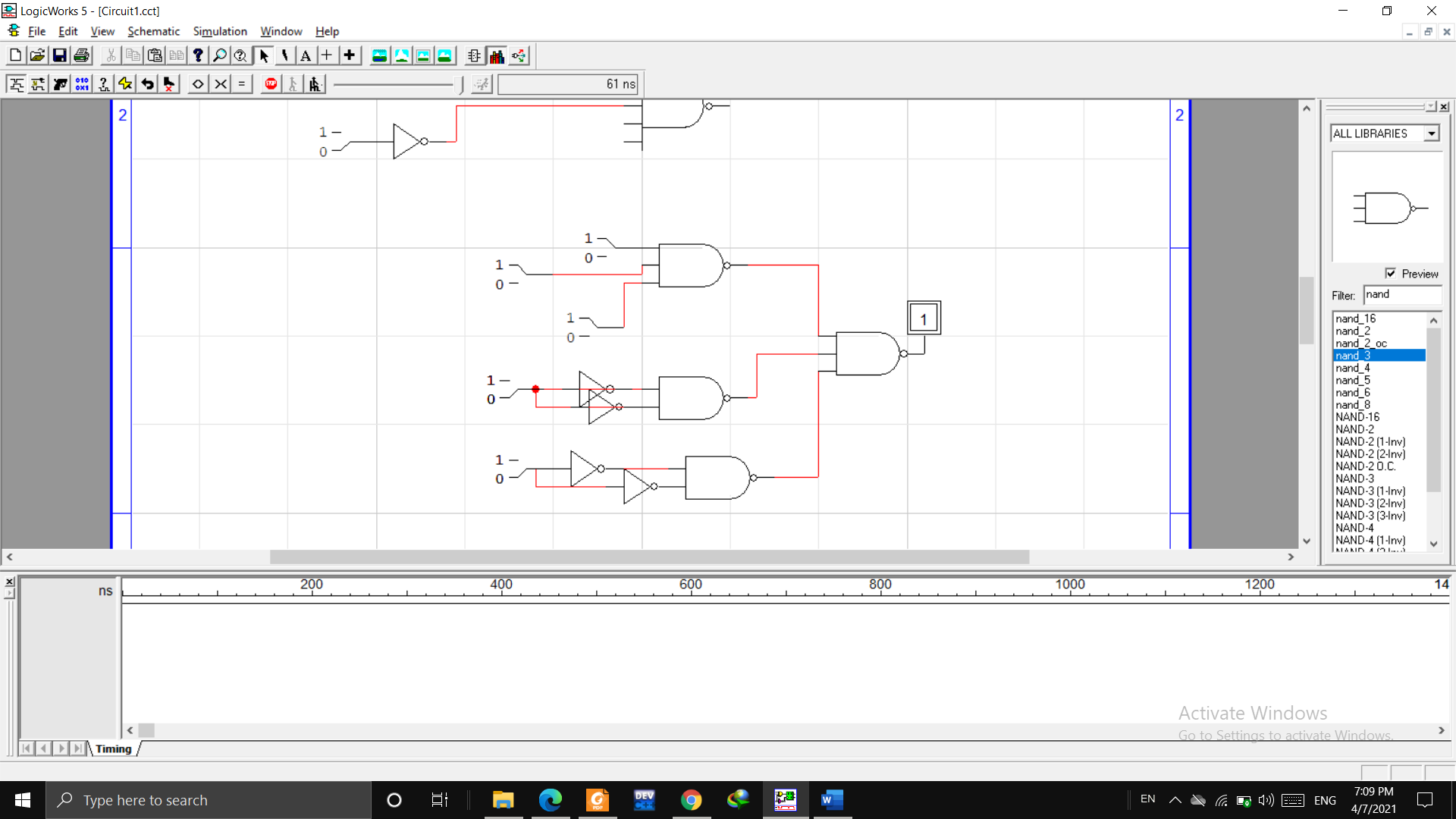
**ROLL\_ NO = 20k-0409**

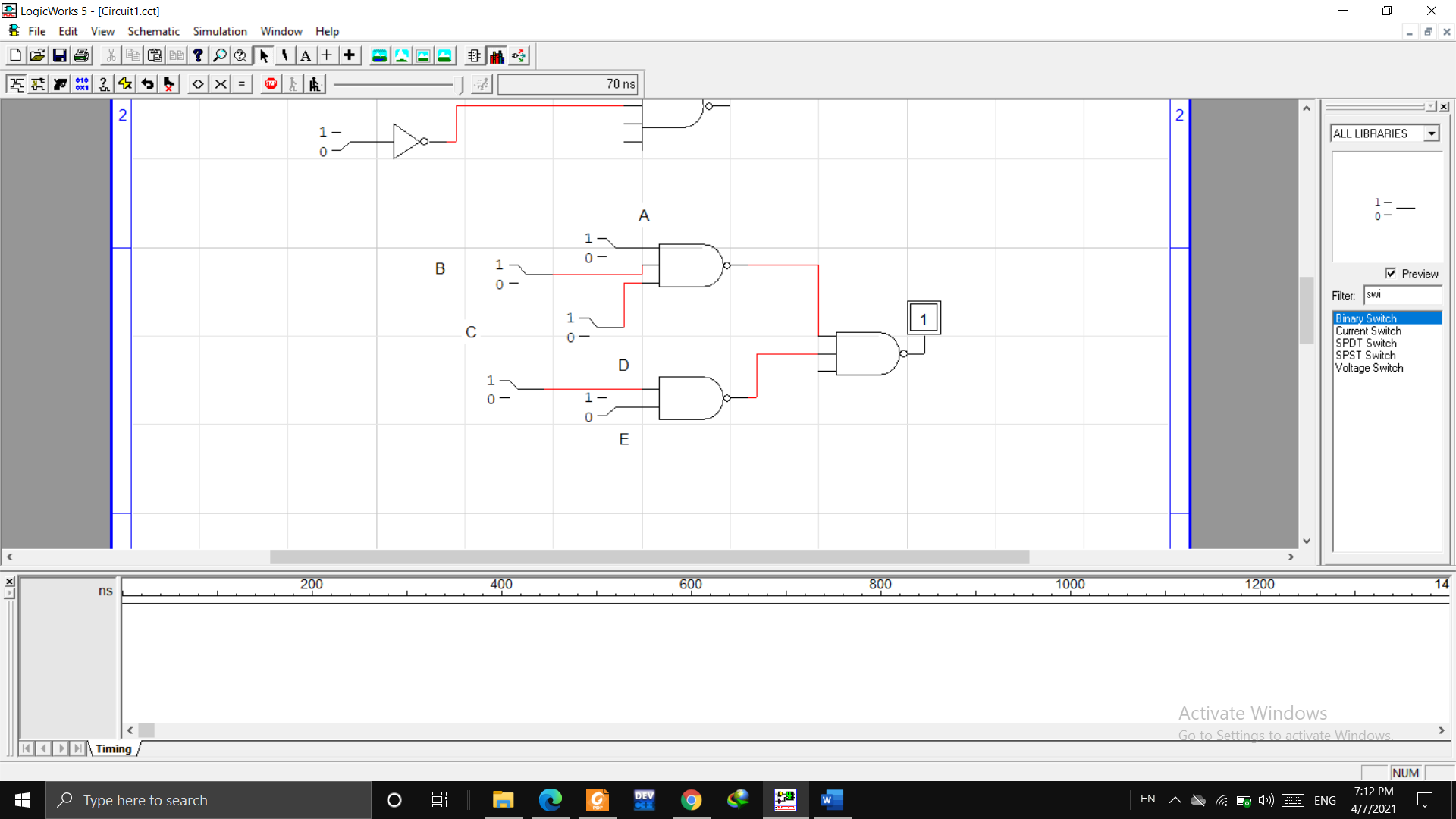
*LAB # 5*

Ques 1.

Design circuit diagram in Logic Works given expressions by using either NAND or NOR gate.

**1. ABC + D' + E' 2. ABC + DE**

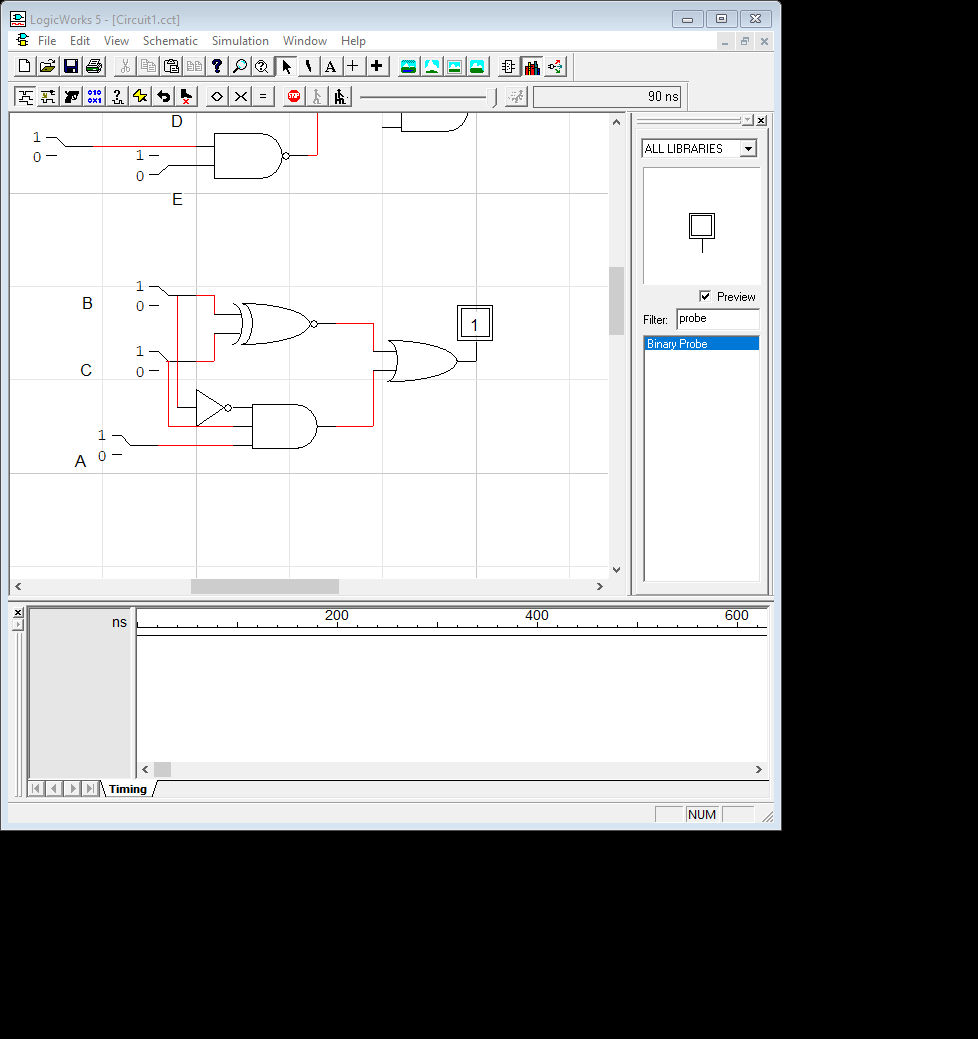
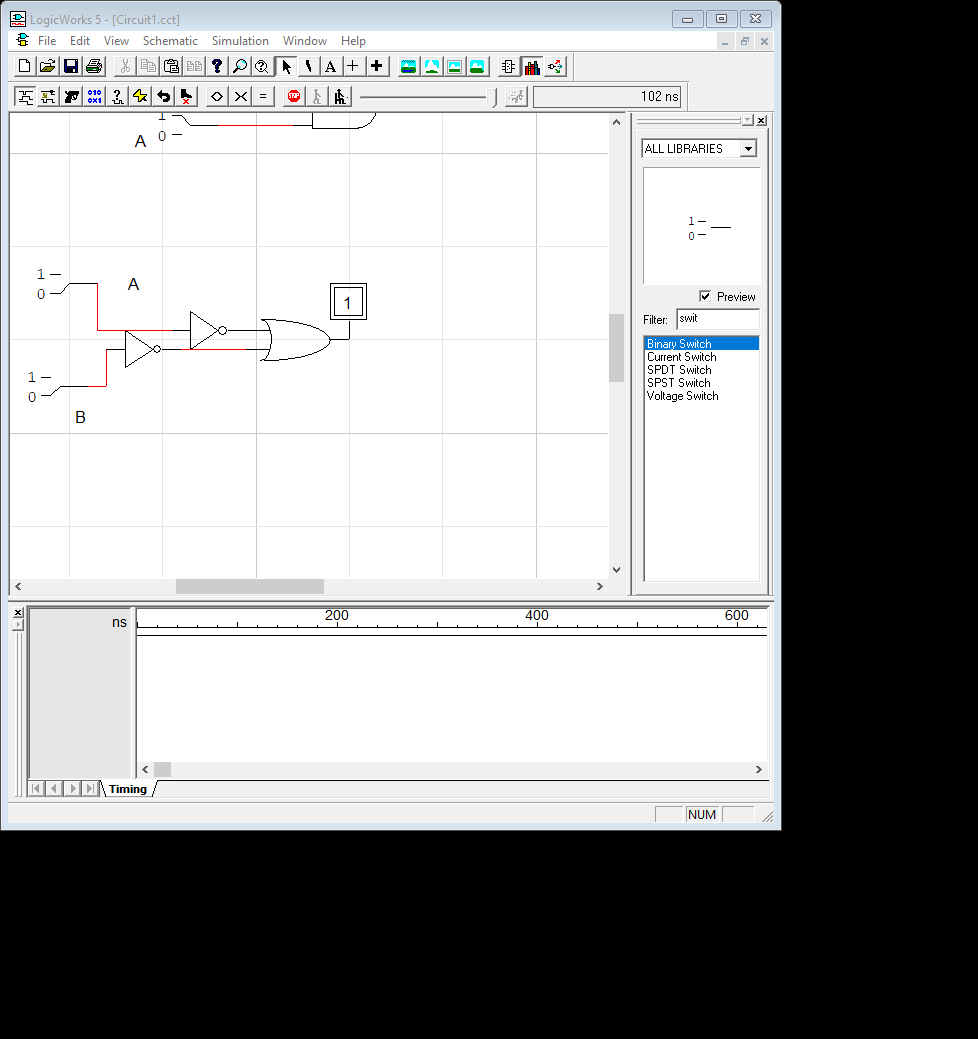
****X = ((ABC + D’ + E’)~)~ = ((ABC)~ . (D’)’ . (E’)’)~ X = ((A.B.C)’ . (D.E)’ )’

****

Ques 2.

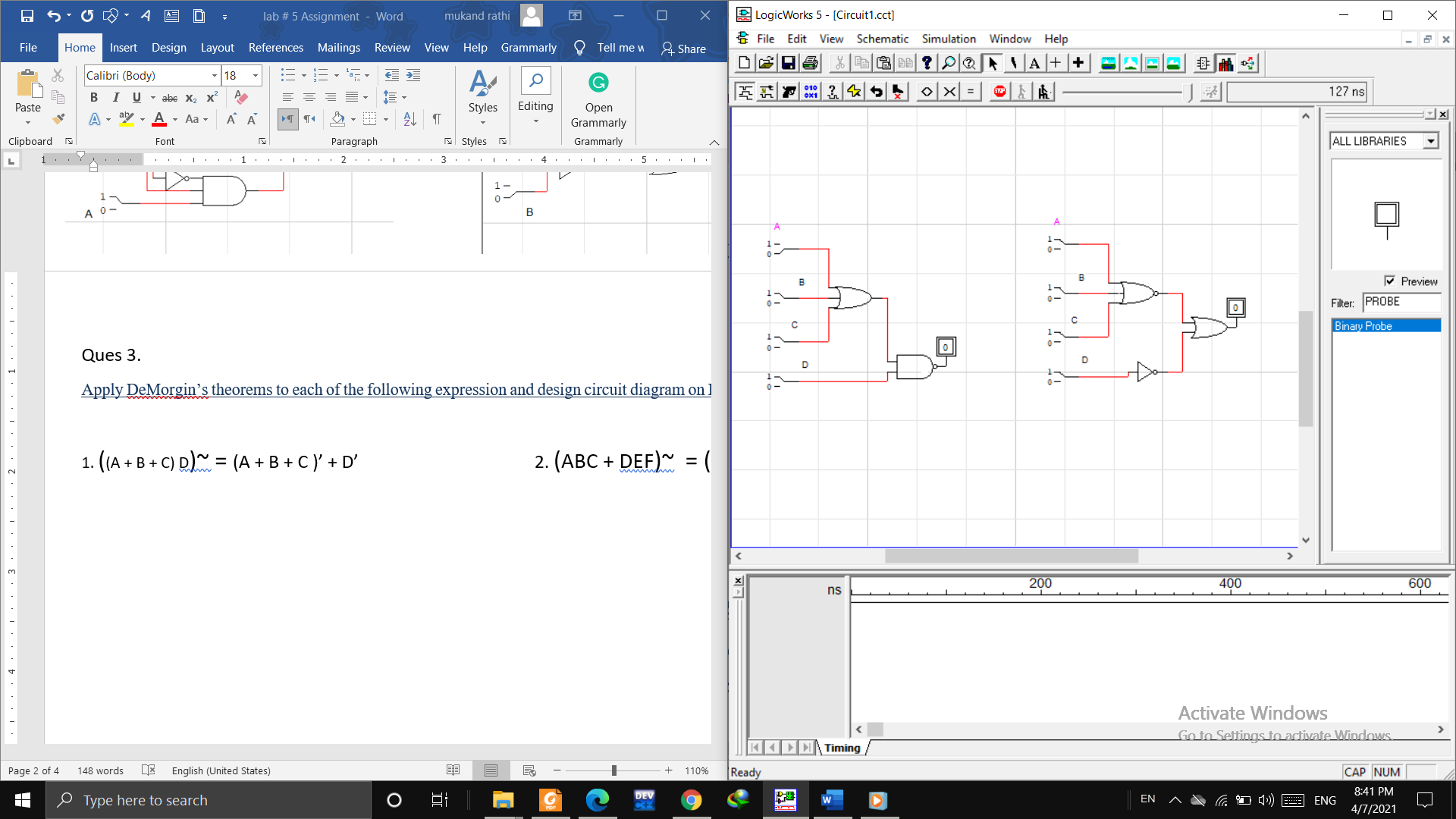
Simplify the following Boolean expression: and design circuit in Logic Works.

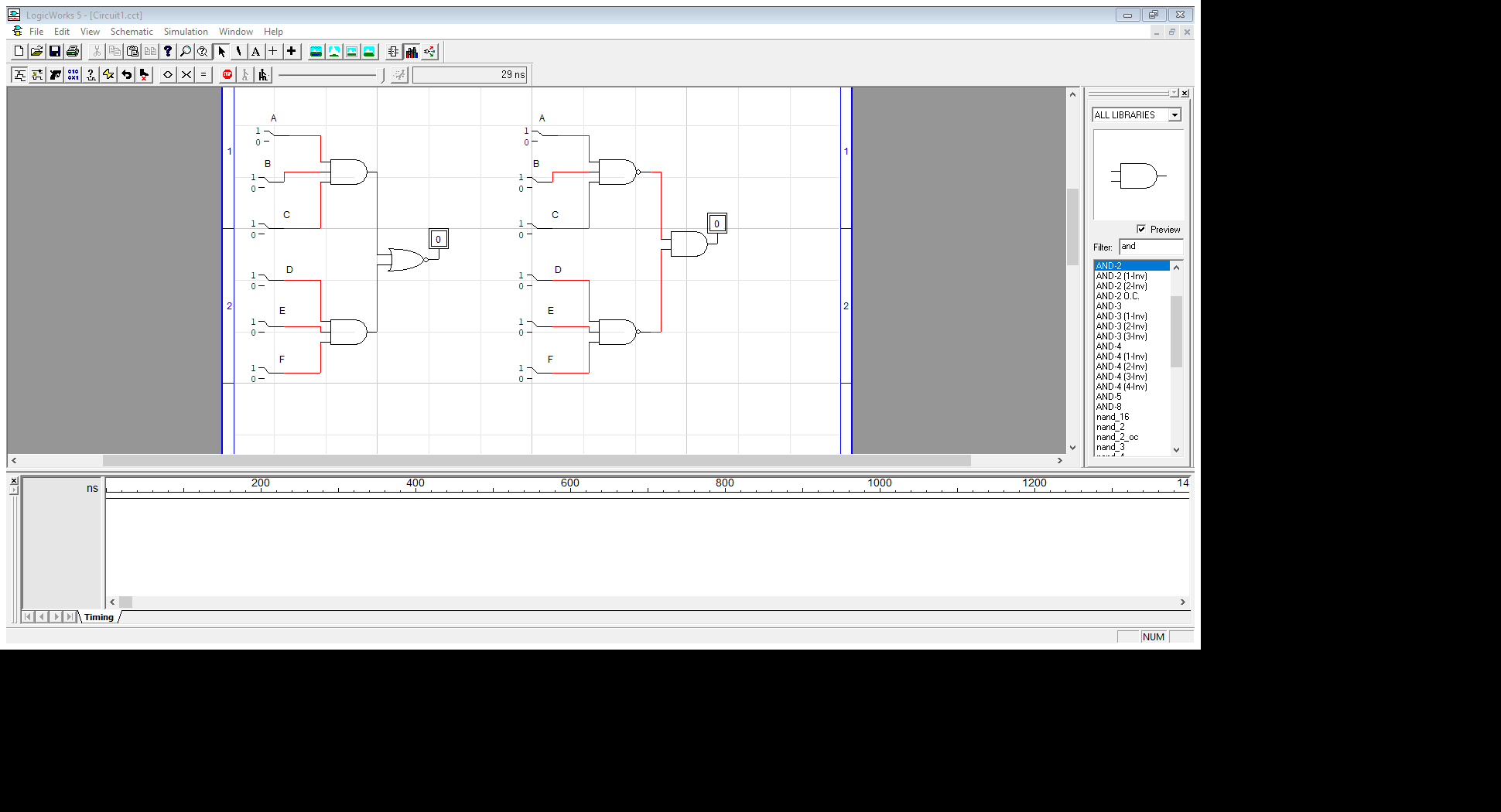
**1. A’BC + AB’C’ + A’B’C’ + AB’C + ABC 2. (AB + AC)’ + A’B’C**

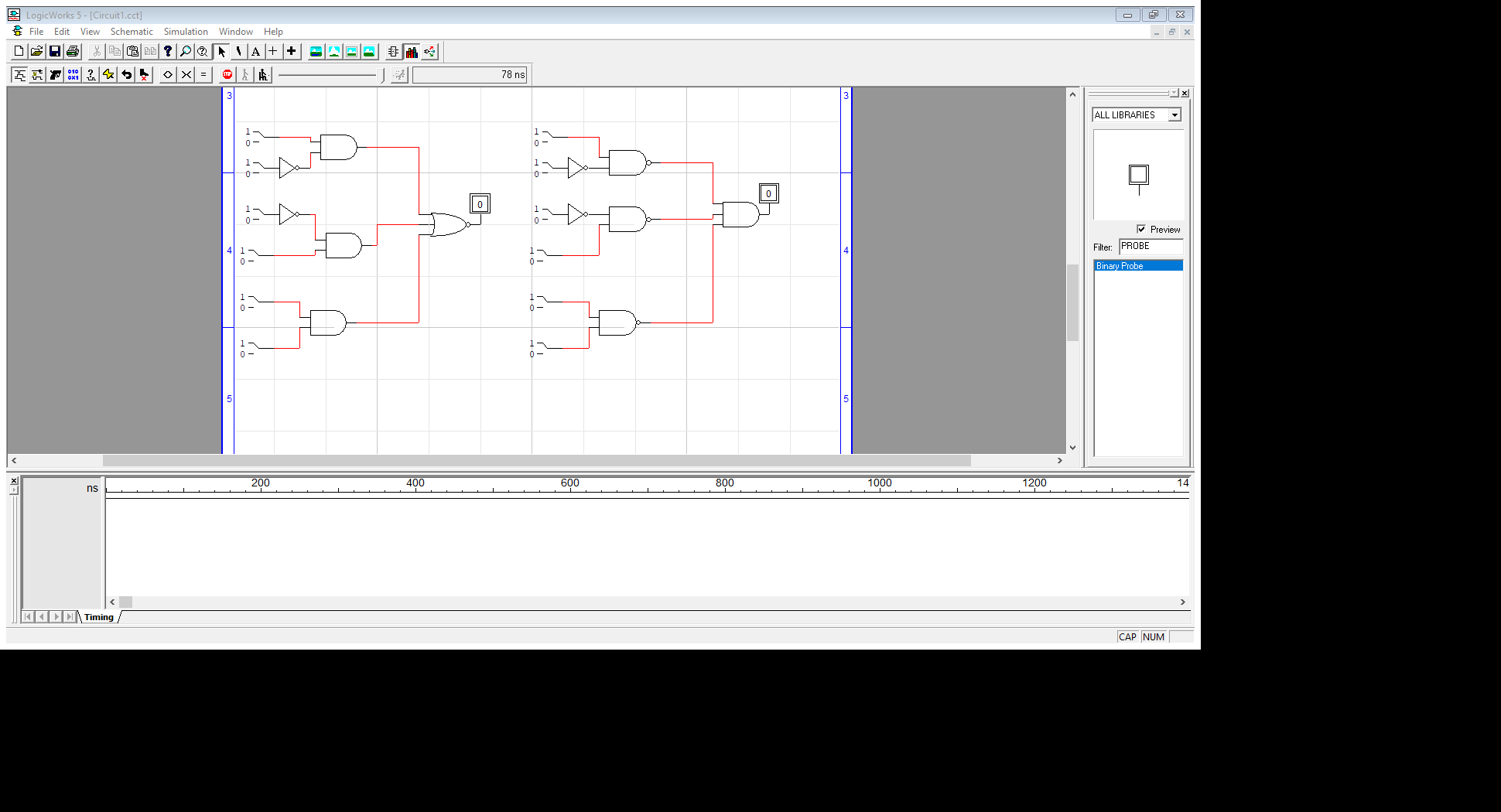
**** X = BC + B’C’ +AB’C = (B + C)’ + AB’C X = A’ + B’

Ques 3.

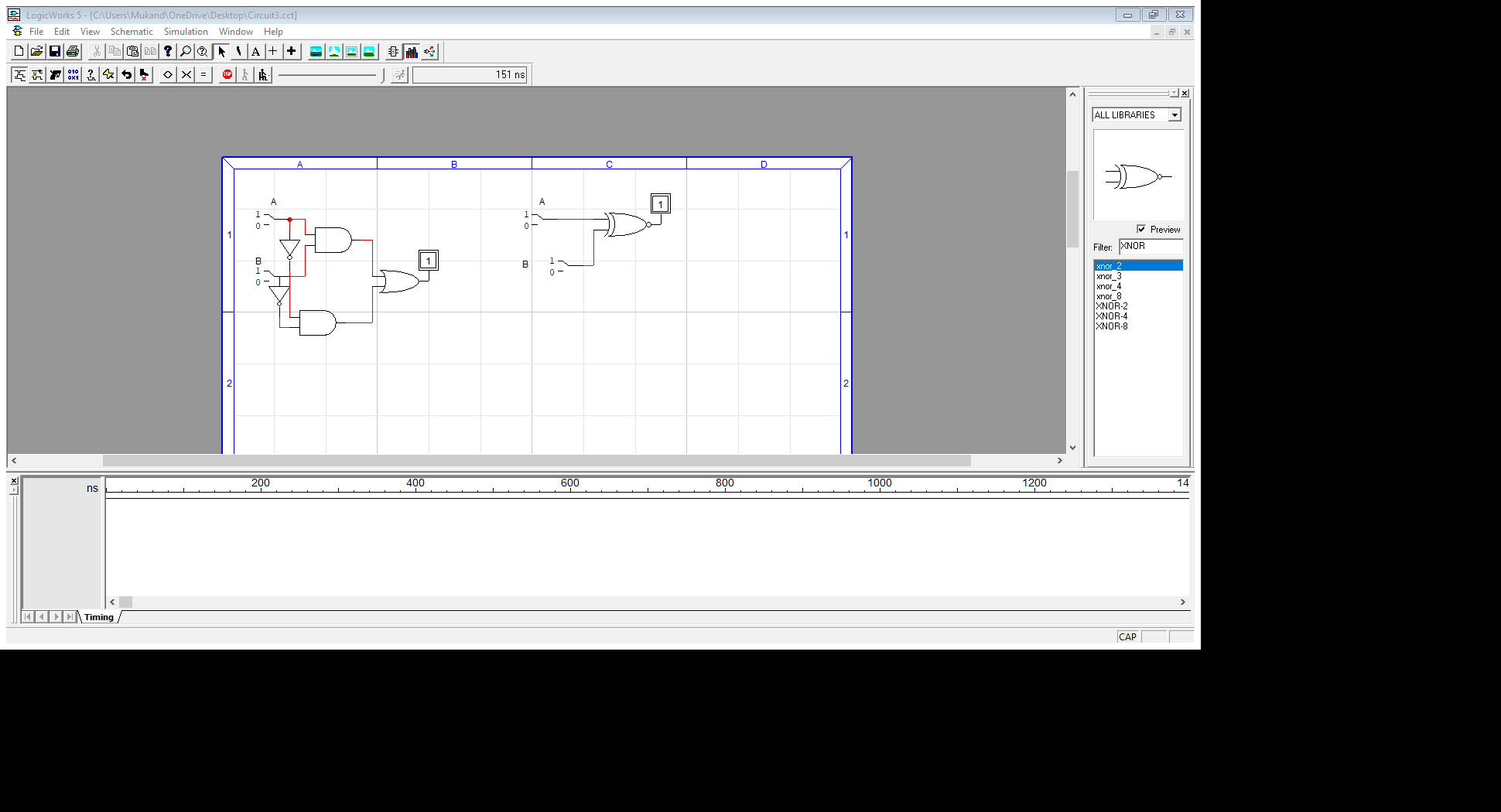
Apply DeMorgin’s theorems to each of the following expression and design circuit diagram on Logic Works

**1. ((A + B + C) D)~ = (A + B + C )’ + D’ 2. (ABC + DEF)~ = (ABC)’ . (DEF)’**



**3. (AB` + C`D + EF) ` = (AB`)`. (C`D) `. (EF)`**

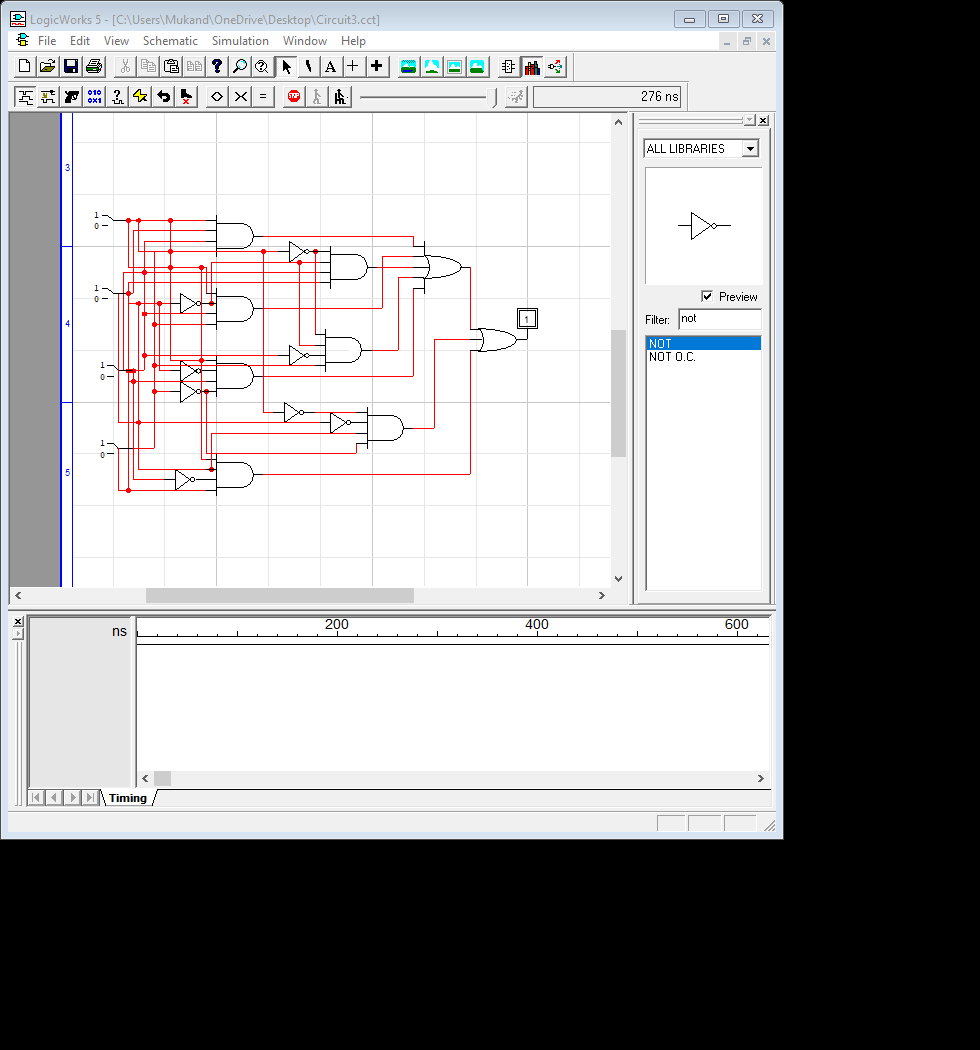
**QUES 4.**The Boolean expression for an exclusive-OR gate is AB’ + A’B. With this as a starting point, use De Morgin’s theorems and any other rules or laws that are applicable to design an expression for the exclusive-NOR gate and design circuit in Logic Works.

 AB` + A`B = (AB` + A’B)` = AB + A’B’ = EXCLUSIVE-NOR GATE

**QUES 5**

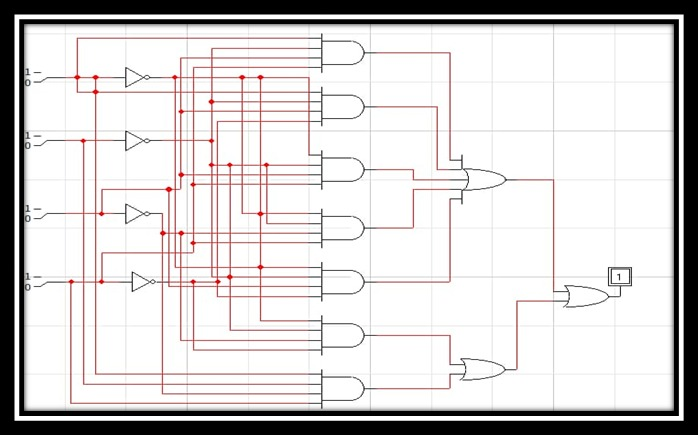
Convert the following Boolean expression into standard SOP form and design circuit diagram in Logic Works:

**AB’C + A’B’ ABC’D = AB’CD + ABCD + AB’CD’ + A’B’CD + A’B’C’D + A B C’ D + A’B’C’D’**

****

QUES 6.

Convert the following Boolean expression into standard POS form and design circuit diagram in  
Logic Works. **AB’C + A’B’ + ABC’D**



Ques 7. **A’B’C + AB’C’ + ABC** Truth table of the expression given below.

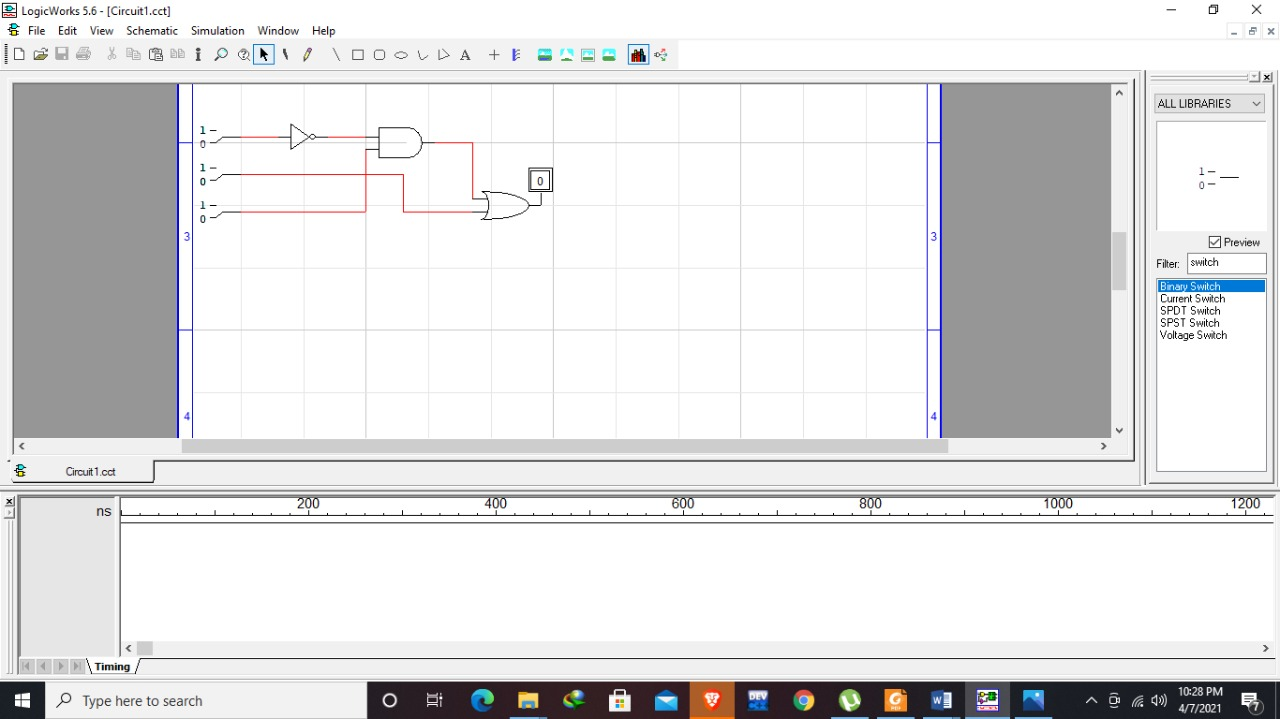
|  |  |  |  |
| --- | --- | --- | --- |
| **A** | **B** | **C** | **X** |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 |

**QUES 8.**

Use a Karnaugh map to minimize the following standard SOP expression and design circuit diagram on Logic Works

**AB’C + A’BC + A’B’C + A’B’C’ + AB’C’**

SIMPLIFIED EXPRESSION: **A‘C + B‘**



QUES 9. Use a Karnaugh map to minimize the following standard POS expression and design circuit  
diagram on Logic Works

(A+B+C) (A+B’+C)(A+B’+C’) (A’+B+C’)(A’+B’+C)

SIMPLIFIED EXPRESSION: = **(A + C ) ( A+B’) (A’+B+C’) (B’+ C)**

